A 36nW CMOS Temperature Sensor with <0.1K Inaccuracy and Uniform Resolution

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Abstract

This paper presents a 36nW high-accuracy subthreshold oscillator-based temperature sensor in 180nm. The proposed super cut-off contention-free (SCCF) delay cell closely mimics the temperature dependency of a single MOS, leading to best-in-class -0.072/+0.082°C (±0.27°C) inaccuracy after 2- (1-) pt calibration. A compact voltage regulator with three native transistors realizes 0.02%/°C line sensitivity and 1mK noise floor. A uniform resolution frequency to digital converter (FDC) keeps the sensing resolution constant across a wide temperature range. In addition to standard testing, the 1-pt calibrated sensor was demonstrated for in-vivo animal body temperature tracking and outperformed off-the-shelf solutions.

Introduction

Across many health monitoring, food, pharmaceutical, and industrial applications, accurate and precise temperature sensing is necessary to track subtle temperature fluctuations. Many ubiquitous systems demand sensors to achieve high accuracy and resolution (<0.1K) with ultra-low power (<1uW) and compact area (<0.1mm^2). Fig.1 visualizes prior arts toward these design targets [1]. BJT-based sensors offer high accuracy and resolution but suffer from a relatively large area and high power even with the latest low-power techniques [2,8]. Resistor-based sensors with high-resolution ADCs offer superior accuracy and precision [3], but the passive components and high-resolution ADCs increase area and power. Alternatively, low-power resistor-based sensors are possible at the cost of accuracy [11,12]. For ultra-low power and compact sensors, the MOS subthreshold current with exponential temperature dependency is attractive [4-7]. Particularly, considering that a high-accuracy reference clock is typically available in wireless edge devices, via embedded real-time clock modules or extracted carrier frequencies from wireless communication [9] and wireless power transfer [10], frequency-based sensors offer ultra-low power and area for an integrated system. However, state-of-the-art MOS sensors [4-7] all require 2-point calibrations and achieve insufficient accuracy and line sensitivity for many applications due to the high PVT sensitivity of a subthreshold MOS. Moreover, these sensors have varying resolutions at different temperatures, complicating data processing and wasting energy. To mitigate these long-standing limitations in MOS-based sensors, we present a novel subthreshold sensor with an SCCF oscillator, a 3T voltage regulator, and a uniform resolution FDC.

Proposed Design

Ideally, the best achievable temperature sensing accuracy happens when we can accurately quantize the current of a single biased MOS. Therefore, our primary goal is to construct a ring oscillator (RO) that better mimics the temperature dependency of a single MOS. In a basic inverter, contention and short circuit current between the pull-up and pull-down paths contaminates the temperature dependency, leading to worse linearity and, more importantly, larger variations of the sensing error across process variations. Since the widely adopted batch-level polynomial curve fitting could compensate for modest systematic non-linearity, a sensor's accuracy is primarily determined by the variation, rather than the absolute linearity, of the frequency vs. temperature curve. The look-ahead differential delay cell in [4] reduces contention in pull-up transition with look-ahead PMOS inputs and makes pull-up transition dominate the overall frequency. However, NMOS leakage currents and the residue charge in the cross-coupled PMOS pair complicate the temperature sensitivity of the pull-up transition, and the pull-down delay also adds to the nonidealities of the overall temperature dependency. Our SCCF delay cell (Fig.2) attempts to alleviate contention in both transition directions. The key idea is to introduce a biased current-limiting footer to a fully differential delay cell, so that node B sees an overshoot during transitions and super-cutoffs M3 in the pull-up branch. Hence, in the pull-up branch, the output is charged by an almost constant and P/N mismatch insensitive current decided by M7. However, generating a bias voltage to bias a conventional footer takes power and adds additional temperature dependencies to the sensor. Leveraging the fully differential oscillation enforced by the cross-coupled PMOS pair, we design an M5/M6 pair driven by the delay cell's outputs to mimic the behavior of a conventional current bias footer. This design not only makes the pull-up transition almost ideal but also controls the discharging current with the equivalent footer and suppresses the PMOS leakage and contention via stacking. As shown by the simulation results in Fig.3, the RO frequency variation is less in the SCCF design than [4]. As a result, the simulated inaccuracy after systematic error fitting is close to the "ideal" scenario of measuring a single NMOS. Meanwhile, the line sensitivity is boosted with a voltage-regulating header using three native NMOS (Fig.4).

To achieve a programmable uniform resolution with an exponentially temperature-dependent sensing frequency and a fixed reference frequency, we propose a uniform resolution FDC structure with an estimation window to quickly determine the proper conversion time at the beginning of each conversion. The principle is to estimate the frequency ratio between sensing and reference clocks in a window of M sensing clock cycles. To avoid the overhead of calculating the division of two counter values directly, we empirically decide to only consider the two most significant valid bits of the reference counter value K as an approximation. With the estimated frequency ratio, we can find the needed number of clock cycles to reach the targeted resolution through a pre-defined look-up table (LUT) stored in a tiny low-power SRAM. Finally, the system stops the conversion once the slower counter of the two reaches the LUT readout value. Detailed counting processes and implementations are illustrated in Fig.5. In a trade-off between estimation accuracy and power/area overheads, two counting bits are chosen for estimation in our uniform resolution FDC.

Measurement Results

Our 180nm CMOS prototype chip (Fig.9) is fabricated in two separate runs to characterize its variation and inaccuracy. The measured 106 sensors across two batches achieved 3σ inaccuracy of -0.072/+0.082°C and ±0.27°C across -20 to 100°C after 2- and 1-point (at 30°C) calibrations for each chip, respectively (Fig.6). This represents the best inaccuracy among all MOS-based ultra-low power temperature sensors. Importantly, with only room-temperature calibration, our sensor achieves ±0.15°C inaccuracy in 0-60°C, which is the widest range that a biomedical application requires. Measurement also confirms the superior uniformity of sensing resolution (<15% variations over -20-to-100°C) at various configured resolution targets, compared with baselines (Fig.7). Thanks to the proposed delay cell and 3T header, the sensor's noise floor reaches 1mK after >500ms conversion time. Its line sensitivity also becomes the best in MOS-based works (Fig.8). To validate the sensor in animal core temperature tracking applications, we performed in-vivo testing in rats with a fully encapsulated sensor (Fig.10). We implanted it along with one of the best off-the-shelf CMOS temperature sensors (TI TMP117) and wireless rodent temperature loggers (DST nanoRF). All three devices track each other relatively well

across the multi-day testing (Fig.11). Our sensor demonstrates higher resolution than nanoRF and superior consistency than TMP117, at orders of magnitude lower power consumption than both commercial devices.

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References: [1] K.A.A. Makinwa, "Smart Temperature Sensor Survey." [2] T. Someya, VLSI 2022. [3] S. Pan, ISSCC 2021. [4] K. Yang, ISSCC 2017. [5] T. Zhong, JSSC 2021. [6] H. Wang, JSSC 2019. [7] T. Someya, JSSC 2019. [8] T-T Zhang, Sensor Journal 2018. [9] A. Alghaihab, ISSCC 2020. [10] Z. Yu, JSSC 2022. [11] A. Jain, TCASII 2021. [12] H. Xin, SSCL 2018.

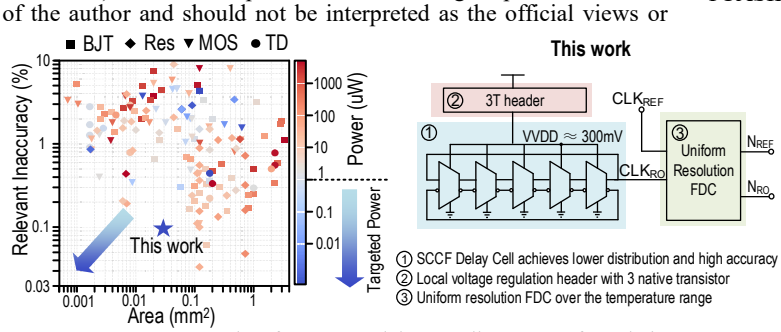

Fig. 1. Targeted performance and the overall structure of our design.

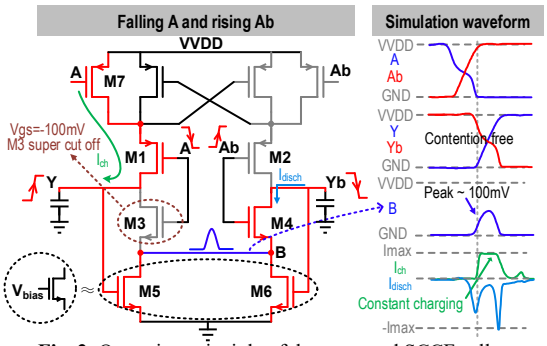

Fig. 2. Operation principle of the proposed SCCF cell.

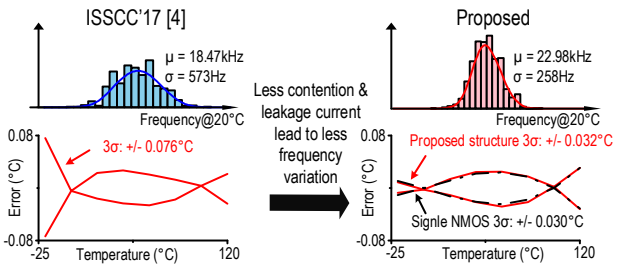

Fig. 3. Mismatch simulation of SCCF cell at room temperature (above) and overall temperature range (bottom).

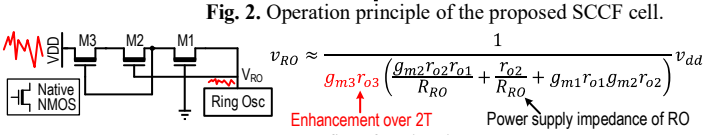

Fig. 4. Benefits of 3T header.

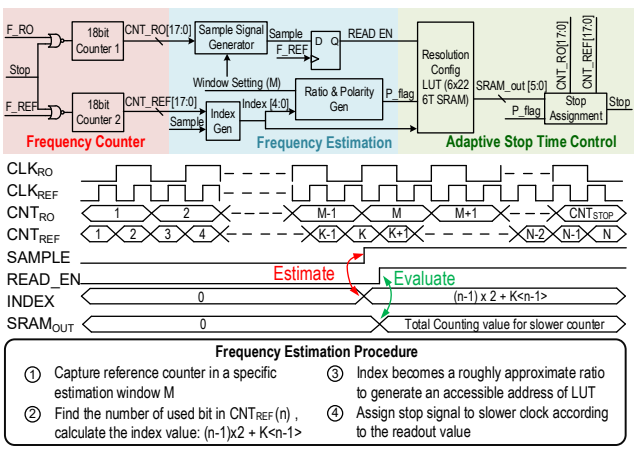

Fig. 5. Implementations and counting process of uniform resolution FDC.

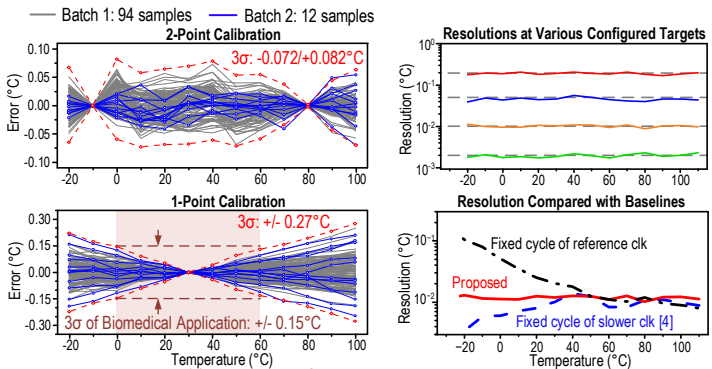

Fig. 6. Measured inaccuracy of 106 samples after 2-/1-point calibration.

Fig. 7. Experimental results of uniform resolution FDC.

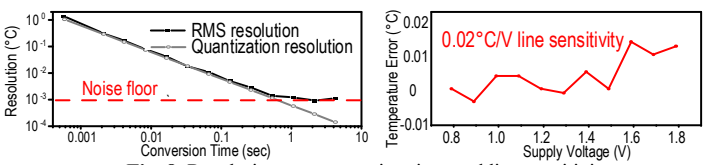

Fig. 8. Resolution vs. conversion time and line sensitivity.

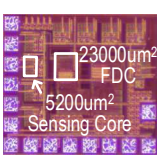

Fig. 9. Die photo.

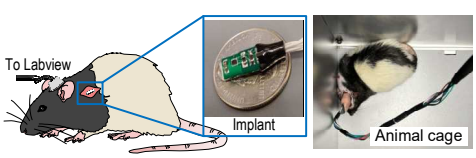

Fig. 10. in-vivo testing setup.

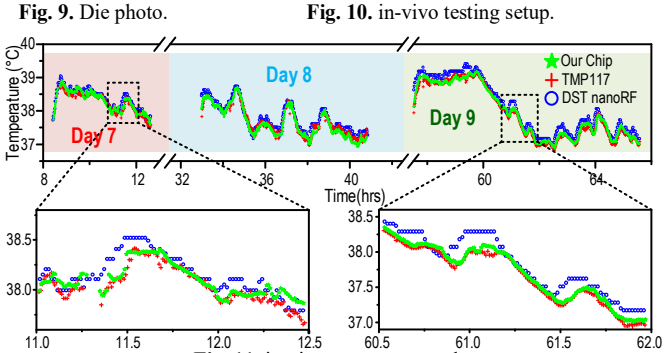

Fig. 11. in-vivo measurement data.

Table I
Comparison with state-of-the-art MOS-based and other sub-uW sensors.

	This Work	JSSC'20 [5]	JSSC'19 [6]	JSSC'19 [7]	ISSCC'17 [4]	VLSI'22 [2]	Sensor'18 [8]	TCASII'21 [11]	SSCL'18 [12]
Technolog(nm)	180	55	65	180	180	180	180	65	65
Type	MOS	MOS	MOS	MOS	MOS	BJT	BJT	RES	RES
Digital Conv.	FDC	FDC	TDC	FDC	FDC	SC Σ Δ	SC Σ Δ	FLL	SAR
Area (um^2)	10700/28200*	1800	630000	74000	8865	58000	180000	470000	60000
Conv.Time (ms)	16	1.31	300	839	8	50	40	10	10
Power (uW)	0.036	9.3	0.0008	0.011	0.075	0.21	0.72	0.3	0.05
Energy (nJ)	0.576	12.2	0.2	9.2	0.6	10.5	28	3.1	0.5
Temp. Range (°C)	-20-100	-40-125	0-100	-20-80	-20-100	-15-85	0-100	-5-95	0-100
1-pt R-IA** (%)	0.45	N/A	N/A	N/A	N/A	0.3	0.36	N/A	2.6
2-pt R-IA** (%)	0.128	0.85	1.56	2.1	0.34	N/A	N/A	3.4	N/A
Resolution (mK)	41	16	300	145	73	15	40	9.8	68
# of Samples	106(2 batches)	64	12	9	16	20	15	14	12
Supply (V)	0.8-1.8	0.8-1.3	0.5	0.7-1.5	1.2	1.2-1.8	1	0.9	0.65, 1
Line Sens.(°C/V)	0.02	5.22	8.4	3.8	0.13	0.07	N/A	2.8	N/A
Res. FOM (pJ*K^2)	0.97	3.12	20.6	190	3.2	2.3	46	0.3	2.3

* FDC with standard counter / FDC with uniform resolution counter ** R-IA = $\frac{\text{Inaccuracy}}{\text{Temperature range}}$ [1]